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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,424	09/28/2000	GURJEET SINGH SAUND	114596-31-0127BS	7407

38492 7590 10/28/2005

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,424	SAUND ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8,9 and 12-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 14-53* is/are allowed.

6)☒ Claim(s) *5,6,8,9,12,13 and 54* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The applicant is advised that the finality of the last office action is cancelled. The amendment dated 9/30/05 has been entered. Action on the merits of the application follows.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scope of meaning of claims 8, and 9 are not clear because each of these claims are dependent of a cancelled claim [claim 11].

Claim Rejections - 35 USC § 103

1. Claims 5,6 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable Colwell (patent No. 5,729,728) in view of over Papworth (patent No. 5,404,473) and Hammond (patent No. 5,638,525).

2. Colwell taught the invention substantially as claimed including a data processing ("DP") system comprising: Decoder (150) (e.g., see fig. 2) that receives a macroinstruction and decodes the macroinstruction into uopcode and [MU] field and microinstruction branch, static bit. Colwell taught the macroinstruction decoding

produced a pattern of microinstructions implementing a basic operation (e.g., see fig.2 and col. 6, line 25- col. 7, line 14 and col. 12, line 61-col.13, line 27). Colwell taught that the decoder transfers stream ops and issues up to three in order uops during each cycle (e.g., see col. 10, lines 27-32). Colwell taught that in the case of a branch instruction outcome was predicted (e.g., see col. 12, lines 7-35).

3. Colwell did not expressly detail (claim 5) that generating a plurality of iterations where a branch was predicted not taken. Papworth however taught the processing of loops including a number of loops specified by a macroinstruction by unrolling the loops into iterations each of which are conditionally executed (e.g., see col. 7, line 2-col. 8, line 25). Papworth also taught a branch Cuop that was predicted not taken of the MS continued to stay in the loop until the MS loop counter was zero or conditional branch Cuop was mispredicted (e.g., see col. 11, lines 2-12).

4. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Colwell and Papworth. Both Colwell and Papworth were directed to toward processing instruction sequences that were conditionally executed. The incorporation of the Papworth teachings of unrolling of loops would have allowed the combined system to more efficiently process sequences of instructions that were repeated by loading unrolled loops into the pipeline and when the end of the iterations occurred fewer pipeline stages would have been required to be flushed or discarded (e.g., see col. 9, lines 3-15 of Papworth).

5. As per claim 5 Colwell taught that microinstruction set architecturally available and a branch instruction available to programs fetched from a memory of the computer

as branch prediction bits for use in processing the microinstructions can be set by a microcode programmer (e.g., see col. 12, lines 19-23). The macroinstructions of Colwell are decoded and in response to the decoding of the macroinstructions the microinstructions are accessed. However Colwell did not specifically detail that the microinstruction set was architecturally exposed to the programs that are fetched from a memory. On the other hand Hammond (patent No. 5,638,525) taught a system with a processor that executes programs that contain CISC and RISC instructions. Note: RISC instructions are microinstructions.

6. One of ordinary skill would have been motivated to incorporate the teachings of Hammond in the system of Colwell and Papworth at least because the added ability to include microinstructions and macroinstructions in programs allows the processor to accepting multiple operating systems and instructions from multiple instruction sets (e.g., see col. 1, lines 49-52 of Hammond). This allows the allow the user or programmer in the Colwell system Papworth system to directly use microinstructions taught by Colwell versus only as determined by the decoding of macroinstructions. This also allows additional flexibility to the programmer or user in the implementation of the combined system to tailor or fine tune or optimize applications.

7. As per claim 6, Colwell, taught an instruction cache (103) and a victim cache (105) (e.g., see fig. 1). Colwell did not however particularize the memory management between external memory and the cache. The use of external memory for storing data and instructions that are not currently being used and providing a memory management to provide at least coherency of the data in the external memory and cache was well

known in the art at the time of the claimed invention. One of ordinary skill would have been motivated to provide a memory management and external memory to allow the system to readily access large amounts of data and instructions as need by the currently running program and the memory management would provide control to determine whether the data in external memory and the cache is valid. On the other hand, Papworth taught fetching instructions from the cache and upon a cache miss fetching instructions from external memory and the system comprising a data cache controller (203) and a bus controller that manages transfers of data and cache coherency (e.g., see col. 4, lines 42-63).

8. As per claim 54 Colwell taught the branch microinstruction is generated carrying a marker indicating that the branch microinstruction defines a boundary (beginning or ending of an iteration of a sequence of microinstructions) (e.g., see col. 10, lines 18-26 of Colwell). When the instruction would have been part of an unrolled loop iteration as taught by Papworth these beginning and ending markers would have provided a boundary between iterations.

9. Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable Colwell (patent No. 5,729,728) in view of over Papworth (patent No. 5,404,473)..

10. Colwell taught the invention substantially as claimed including a data processing ("DP") system comprising: Decoder (150) (e.g., see fig. 2) that receives a macroinstruction and decodes the macroinstruction into uopcode and [MU] field and microinstruction branch, static bit. Colwell taught the macroinstruction decoding

produced a pattern of microinstructions implementing a basic operation (e.g., see fig.2 and col. 6, line 25- col. 7, line 14 and col. 12, line 61-col.13, line 27). Colwell taught that the decoder transfers stream ops and issues up to three in order uops during each cycle (e.g., see col. 10, lines 27-32). Colwell taught that in the case of a branch instruction outcome was predicted (e.g., see col. 12, lines 7-35).

11. Colwell did not expressly detail (claim 13) that generating a plurality of iterations where a branch was predicted not taken. Papworth however taught the processing of loops including a number of loops specified by a macroinstruction by unrolling the loops into iterations each of which are conditionally executed (e.g., see col. 7, line 2-col. 8, line 25). Papworth also taught a branch Cuop that was predicted not taken of the MS continued to stay in the loop until the MS loop counter was zero or conditional branch Cuop was mispredicted (e.g., see col. 11, lines 2-12).

12. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Colwell and Papworth. Both Colwell and Papworth were directed to toward processing instruction sequences that were conditionally executed. The incorporation of the Papworth teachings of unrolling of loops would have allowed the combined system to more efficiently process sequences of instructions that were repeated by loading unrolled loops into the pipeline and when the end of the iterations occurred fewer pipeline stages would have been required to be flushed or discarded (e.g., see col. 9, lines 3-15 of Papworth).

13. As per claim 13, Papworth taught ceasing to generate iterations when a condition of the macroinstruction is detected (e.g., see col. 7,line 24-col. 8,line 25) that comprises

a branch mispredict (e.g., see col. 9, lines 3-15) as when the number of iterations is too many the extra iterations are executed as noop operations.

14. As per claim 13 Colwell taught the branch microinstruction is generated carrying a marker indicating that the branch microinstruction defines a boundary (beginning or ending of an iteration of a sequence of microinstructions) (e.g., see col. 10, lines 18-26 of Colwell). When the instruction would have been part of an unrolled loop iteration as taught by Papworth these beginning and ending markers would have provided a boundary between iterations.

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colwell and Papworth as applied to claim 13 above, and further in view of Hammond (patent No. 5,638,525).

16. As per claim 12 Colwell taught that microinstruction set architecturally available and a branch instruction available to programs fetched from a memory of the computer as branch prediction bits for use in processing the microinstructions can be set by a microcode programmer (e.g., see col. 12, lines 19-23). The macroinstructions of Colwell are decoded and in response to the decoding of the macroinstructions the microinstructions are accessed. However Colwell did not specifically detail that the microinstruction set was architecturally exposed to the programs that are fetched from a memory. On the other hand Hammond (patent No. 5,638,525) taught a system with a processor that executes programs that contain CISC and RISC instructions. Note: RISC instructions are microinstructions.

17. One of ordinary skill would have been motivated to incorporate the teachings of Hammond in the system of Colwell and Papworth at least because the added ability to include microinstructions and macroinstructions in programs allows the processor to accepting multiple operating systems and instructions from multiple instruction sets (e.g., see col. 1, lines 49-52 of Hammond). This allows the allow the user or programmer in the Colwell system Papworth system to directly use microinstructions taught by Colwell versus only as determined by the decoding of macroinstructions. This also allows additional flexibility to the programmer or user in the implementation of the combined system to tailor or fine tune or optimize applications.

18. Applicant's arguments with respect to claims 5,6,8,9,12, and 13 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

19. Claims 1,14-53 are allowed.

20. Claims 3,4, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liu (patent No. 6,088,793) disclosed a system for branch execution on a multiple-instruction-set architecture where CISC instructions are decoded into RISC instructions for execution (e.g., see col. 3, lines 38-58).

Knebel (patent No. 6,820,190) disclosed a system for decomposing microinstructions into microinstructions and disclosed that instructions of the RISC instruction set architecture are called microinstructions (e.g., see col. 1, lines 15-21).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER